REMARKS

Claims 28-36 and 38-45 are presently pending in the application. Favorable reconsideration of the application is earnestly requested.

Withdrawal of the objection to the specification under 35 U.S.C. § 112 in light of the amendments made to pages 8, 9 and 10 is requested.

Withdrawal of the rejection of claims 32-35 and 43 under 35 U.S.C. § 112 as failing to allegedly have proper antecedent basis for the claimed subject matter is requested. The Office Action misapplies claim 32 to the subject matter of Figs. 1C, 4B, 6D and 8D. However, claim 32 is directed to the embodiment illustrated in Figs. 10A-10K, 12A-12E and 14A-14E. These figures and the corresponding description in the specification disclose (particularly with respect to Fig. 10K) a gate electrode and a first conductive film 35, 46 which provides the support for the claim.

Withdrawal of the rejection of claims 32-35 and 43 under 35 U.S.C. § 112 is requested. The claims have been amended to more clearly recite the subject matter which is disclosed in the application. Claim 42 (which now includes the subject matter of cancelled claim 43) has been amended to provide support for the insulating interlayer. Fig. 10D refers to an insulating interlayer (see page 29 of the specification) which is later filled with an aluminum alloy film 51 (see page 31 of the specification).

Withdrawal of the rejection of claim 43 is requested in that claim 43 is now cancelled.

Withdrawal of the rejection of claims 42-45 under 35 U.S.C. § 112 is requested. Claim 42 has been amended to include antecedent basis for the insulating interlayer.

Withdrawal of the rejection of claims 36 and 42 under 35 U.S.C. § 102(e) as being anticipated by Schoenfeld et al. (U.S. Pat. No. 6,010,932) is requested. The rejected claim 36 provides for a hole, illustrated more particularly in Figs. 12B and 13 as a cylindrical opening 54 in a recess 49. In accordance with the structure of claim 36, the capacitance of the dielectric film 45 made from an ONO film can be increased by the substantially cylindrical opening 54.

Turning now to Schoenfeld et al., recesses such as 144, do not constitute a hole, or opening such as illustrated with respect to Figs. 12B and 13 of the present application, and which are included in rejected claim 36. Further, claim 42 also requires that there be a through hole, exposing the insulating layer. The insulating interlayer functions as a stopper, permitting the polysilicon film 41 to be patterned. Further, the aforesaid feature of obtaining a superior effect by increasing the capacitance of the dielectric film using this substantially cylindrical opening 54 is obtained, a feature which is not shown in Schoenfeld et al. Since it is not seen were Schoenfeld et al. provides for the hole extending through the conductive film until the insulating layer is exposed in a first opening of mask pattern, Schoenfeld et al. cannot anticipate the invention.

Withdrawal of the rejection of claims 38 and 39 under 35 U.S.C. § 103(a) as being unpatentable over Komori et al. (U.S. Pat. No. 5,300,802) in view of Wolf et al. (Silicon Processing For The VLSI Era, Vol. 1) is requested. As noted in the Office Action, Komori et al. does not disclose the step of patterning the first conductive layer. The secondary reference to Wolf et al. as is suggested in the Office Action, discloses a conventional patterning of a film using photolithography where a mask is formed, and recesses are formed, as distinguished from an opening was created, until the element isolation structure is exposed in the first and second openings. The feature of using the element isolation structure as a stopper to divide the first conductive film below the first opening, and simultaneously forming a hole below the second opening, does not appear to be disclosed in either reference. Accordingly, it is not seen how the combination of references would yield or disclose the subject matter of the present application.

Withdrawal of the rejection of claim 40 under 35 U.S.C. § 103 is requested, in that claim 40 is dependent on claim 38 and carries all the limitations thereof.

Withdrawal of the rejection of claim 41 under 35 U.S.C. § 103 is requested, in that claim 41 is dependent on claim 38 and carries all the limitations thereof.

Withdrawal of the rejection of claim 43, which is now cancelled in favor of claim 42 is requested. As noted previously, the Schoenfeld et al. reference discloses a recess 144 in the surface of an insulating interlayer. However, the present invention requires

that a hole 54 be provided using the insulating layer as a stopper. The through hole as shown in Fig. 12B insures patterning of the polysilicon film 41 securely. The cylindrical opening 54 provides an increased capacitance which is disclosed in the Schoenfeld et al. reference.

Withdrawal of the rejection of claim 44 under 35 U.S.C. § 103 is requested. Claim 44 is dependent on claim 42 and carries all the limitations thereof.

Withdrawal of the rejection of claim 45 under 35 U.S.C. § 103 is requested. Claim 45 is dependent on claim 42 and carries all the limitations thereof.

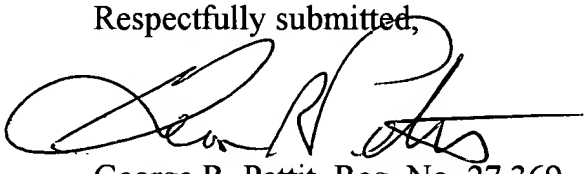
In view of the foregoing, it is respectfully requested that favorable reconsideration be provided.

In view of the above, consideration and allowance are, therefore, respectfully solicited.

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

The Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to CBLH Deposit Account No. 22-0185.

Respectfully submitted,



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MARKED-UP REVISIONS

IN THE SPECIFICATION:

Pages 6-7, paragraph 2 should read

A method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming an insulating film on the semiconductor substrate in the element active region, the third step of forming a first conductive film on an entire surface of the semiconductor substrate including the insulating film and the element isolation structure, the fourth step of forming a mask pattern having first and second openings on the first conductive film, the fifth step of etching the first conductive film until the element isolation structure is exposed in the first opening by using the mask pattern as a mask, thereby dividing the first conductive film, and simultaneously forming a recess in the second opening [by leaving] having the first conductive film [behind] on a bottom of the recess, the sixth step of forming a dielectric film so as to cover a surface of the first conductive film, and the seventh step of forming a second conductive film on the dielectric film [and opposing] opposite [second conductive film to] the first conductive film [through] and separated by the dielectric film.

Pages 7-8, paragraph 1 should read

Another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming a gate insulating film and a gate electrode in the element active region, the third step of doping an impurity into the second substrate to form a pair of impurity diffusion layers in surface regions of the semiconductor substrate on two sides of the gate electrode, the fourth step of forming a first conductive film electrically connected to one of the impurity diffusion layers, the fifth step of forming a mask pattern having at least

first and second openings on the first conductive film, the sixth step of etching the first conductive film by using the mask pattern as a mask, thereby dividing the first conductive film in the first opening, and simultaneously forming a recess in the second opening [by leaving] where the first conductive film [behind] is on a bottom of the recess, the seventh step of forming a dielectric film so as to cover a surface of the first conductive film, and the eighth step of forming a second conductive film on the dielectric film [and opposing] opposite the second conductive film [to the first conductive film through] and separated by the dielectric film.

Pages 8-9, paragraph 2 should read

Still another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming an insulating film on the semiconductor substrate in the element active region, the third step of forming a first conductive film on an entire surface including the insulating film and the element isolation structure, the fourth step of forming a mask pattern having at least first and second openings on the first conductive film, the fifth step of etching the first conductive film until the element isolation structure is exposed in the first and second openings by using the mask pattern as a mask, thereby dividing the first conductive film below the first opening, and simultaneously forming a hole extending through the first conductive film below the second opening, the sixth step of forming a dielectric film so as to cover the first conductive film, and the seventh step of forming a second conductive film on the dielectric film opposite the first conductive film and separated by the dielectric film.

Page 10, paragraph 1 should read

In the semiconductor device of the present invention, a recess or a hole is formed in the charge storage film. Therefore, the area of the dielectric film can be increased to increase the charge storage amount. Especially when a hole is formed, the charge storage

film and the conductive film can be opposite to each other and separated by the dielectric film within the range from the lower surface to the upper surface of the hole. Consequently, the charge storage amount can be effectively increased.

IN THE CLAIMS:

42. (Amended) A method of fabricating a semiconductor substrate, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate oxide film and a gate electrode on said semiconductor substrate in said element active region;

the third step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming an insulating interlayer on an entire surface of said semiconductor substrate [a first conductive film electrically connected to one of said impurity diffusion layers];

the fifth step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed [mask pattern having at least first and second openings on said first conductive film];

the [fourth] sixth step of forming a first conductive film on said insulating interlayer which fills said hole electrically connected to one of said impurity diffusion layers covering;

the [fifth] seventh step of forming a mask pattern having at least first and second openings on said first conductive film;

the [sixth] eighth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a hole extending through said first conductive film below

said second opening, said first conductive film is etched until said insulating interlayer is exposed in said first opening;

the [seventh] ninth step of forming a dielectric film so as to cover a surface of said first conductive film; and

the [eight] tenth step of forming a second conductive film so as to cover said dielectric film [and] opposing said first conductive film through said dielectric film.

44. (Amended) A method according to claim 42, further comprising, between the [fourth] sixth and [fifth] seventh steps[, the ninth] step of planarizing said first conductive film by polishing.